Approved 3/17/05 JM

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IN THE ABSTRACT:

Please amend the abstract of the disclosure as follows:

A time shift circuit for changing a delay timing of a portion of a test pattern for testing a semiconductor device. The time shift circuit includes a multiplexer for selectively producing delay value data indicating a value of time shift in response to a shift command signal, a vernier delay unit for producing timing vernier data based on the delay value data selected by the multiplexer, and a timing generator for generating a timing edge for the specific portion of the test pattern based on the timing vernier data from the vernier delay unit. The shift command signal sets either a normal mode where predetermined delay value data is selected by the multiplexer or a time shift mode where delay value data for shifting the timing edge in real time is selected by the multiplexer.